APPENDIX II Marked-up Version of the Amended Claims

- 2. (Amended) The ESD protection circuit of claim 1, further comprising a lateral shunt resistor coupled between the cathode and the [lateral] external triggering device.
- 4. (Amended) The ESD protection circuit of claim 3, wherein a surface area [over a non high-doped region and] between the respective first and second high-doped regions of the first and second bipolar transistors are blocked from shallow trench isolation.
- 15. (Amended) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:
 - a SCR further comprising:
 - a substrate;
 - a N-well and an adjacent P-well formed in said substrate and defining a junction therebetween;
 - at least one N+ doped region in said P-well and coupled to ground;
 - a P+ doped region in said N-well and coupled to a pad of said protected circuitry;
 - at least one P+ doped trigger tap disposed proximate to at least one N+ doped region in said P-well; and
- [a] <u>an external on-chip</u> triggering device coupled to the SCR, wherein one terminal is coupled to the pad and a second terminal is coupled to the trigger tap.
- 17. (Amended) The ESD protection circuit of claim 15, wherein a surface area [over a non-high-doped region and] between the at least one N+ doped region and the P+ doped region is shallow trench isolation blocked.

- 24. (Amended) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:
 - a SCR further comprising:
 - a substrate;
 - a P-well and an adjacent N-well formed in said substrate and defining a junction therebetween;
 - at least one P+ doped region dispersed in said N-well;
 - a N+ doped region dispersed in said P-well and coupled to ground;
 - at least one N+ doped trigger tap disposed proximate [and between] the at least one P+ doped region in said N-well; and
- a PMOS transistor triggering device coupled to the SCR, wherein [the] <u>a</u> drain is coupled to ground and [the] <u>a</u> source is coupled to the trigger tap; the at least one P+ doped region is further coupled to a pad; the source is further coupled to the pad via a shunt resistor; and the pad is further coupled to said protected circuitry.